IN THE SPECIFICATION:

Please amend the paragraph beginning at page 11, line 19, as follows.

In a further variation, the global time signal, T, supplied by the global cycle counter 310 can be cascaded from one cache line counter to another (or from one group of counters to another), to distribute the "writing back" of "dirty" cache lines in a write-back cache implementation. Thus, a given cache line (or group of cache lines) writes back to main memory, if necessary, before passing the global time signal, T, to the next cache line (or group of cache lines). In this manner, the cascading of the distribution of the global time signal, T, spreads out the decay associated with a single count from the global counter 310.

IN THE TITLE:

Please amend the title as indicated below:

Method and Apparatus for Reducing Leakage Power in Cache Memories Based on Cache Line Decay